

## ABSTRACT OF THE DISCLOSURE

A manufacturing method of manufacturing a semiconductor device having a plurality of wiring layers. The method includes the steps of forming a wiring by a first wiring layer as a pattern by dividing a desired pattern into a plurality of patterns, connecting the divided patterns, and exposing them, wherein a position of the connection is formed in parallel with the wiring which is formed by the first wiring layer, and forming a wiring by a second wiring layer having an area which intersects the connecting position by a batch processing of exposure.